REMARKS

Claims 4, 5, 12-14, 18, 19, 21, 27 and 28 have been rejected under 35 USC 112, second paragraph. The claims have been amended accordingly.

Claims 1-9, 12-14 and 27-28 have been rejected under 35 USC 102(b) as anticipated by Hirano. The rejection is respectfully traversed.

Simply stated, Hirano fails to disclose a circuit comprising a first switching element (ST2), a second switching element (ST1), an amplifier (SC1-SD1) and a capacitor (CS1) as found, for example, in Fig. 26. In fact, SC1-SD1 in Hirano discloses "a second electrode is connected to a supply voltage via SC1, and also connected to the ground voltage via SD1" as stated in column 1, lines 33-35.

More specifically, the following patentable distinctions may be found between the applied prior art and the claimed invention, with reference to the attached exemplary figures. In Hirano, connections of the first switching element ST2 are such that one end is connected to node N10 and the other is permanently connected to capacitor CS2. In the claimed invention, connections of first switching element S1 are such that one end is connected to terminal H and the other end is connected to a signal source (Fig. A1 & A2), an output of an amplifier (Fig. A3) or to another switch connected to analog ground (Fig. A4). Additionally, in Hirano, the structure must use at least 5 capacitors and 6 switching elements in order for it to work. Advantageously, in the claimed invention, only 1 capacitor and 2 switching elements are necessary.

Turning to clocking of switches, in Hirano, clocking of the switches SC1, ST1, ST2, ST3, ST4 and SD1 is by non-overlapping clock signals, whereas, in the claimed invention, clocking of the switches S1 and S2 is by two phase-shifted clock signals.

During operation of the circuit, Hirano discloses a DC charge transfer from one capacitor to another capacitor and to another capacitor for the memory-cell-array operation (see, for example, Figs. 1-6), whereas, in the claimed invention, charge injection charges and clock feed-through

charges flow into the node that is connected to the input of an amplifier (Figs. A1-A4). Additionally, in Hirano, node N10 is switched between the power supply via SC1 and ground via SD1 so as to charge CR1 to the power supply or to discharge CR1 to ground (see, for example, col. 1, lines 33-35). In the claimed invention, on the other hand, none of the switch elements are switched between a power supply and ground, and none of the capacitor is charged to the power supply or discharged to ground.

For applications of the circuit, Hirano discloses an application on a **digital** circuit, as in refreshing of **memory-cell-arrays** (see, Abstract, lines 16-17, "Moreover, this invention can be applied to refresh operation of the identical memory-cell-array."), whereas the claimed invention is applied to switched-capacitor **analog** circuit, **switched-capacitor signal processing circuits** (Figs. A1-A4).

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 529002000100. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

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Respectfully submitted,

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